REMARKS

Claims 1-8, 10 and 11 stand rejected under §103 as being obvious in view of Peng et al. et al. (U.S. Patent No. 5,895,223) in view of Przybysz (U.S. Patent No. 4,353,779). The rejection is respectfully traversed because neither Peng et al. nor Przybysz, alone or in combination, disclose or suggest at least the step of forming porous Group III-V by etching a Group III-V surface in a HF and oxidant solution, as in claim 1. Applicants request reconsideration and withdrawal of the rejection.

All of the cited references are merely directed to material removal processes, and not to the formation of porous Group III-V material. Further, the Examiner has only cited references disclosing metal contacts and structures, which are not thin discontinuous layers of metal. The Examiner has failed to make a prima facie case of obviousness because there is not even a single applied reference that is directed to the formation of porous Group III-V material. None of the references applied produce porous material, each instead performs an etch to pattern a semiconductor quality Group III-V layer without altering the nature of the layer. The structures may have metal contacts and other common device features, but none of the references disclose a thin discontinuous layer of metal that is deposited on a Group III-V material surface.

There are also additional defects in the rejection. The Office Action states that Przybysz suggests a modification of Peng et al. to use the etching solution of Przybysz on a nitride chip with partially metal-coated electrode as part of a porous Group III-V formation process. No such suggestion is provided by the teachings of Przybysz. The overall

approaches of both Peng et al. and Przybysz are distinct from what is presently claimed, mainly the formation of porous Group III-V.

Peng et al. is not directed to the formation of porous Group III-V, but is directed to a wet-etching technique for etching nitride in which the rate of etching, the roughness of the etching surface, and the uniformity of the etching depth is controlled (col. 2, lns. 12-15). Accordingly, the reference discloses the steps of coating an electrode on the nitride chip, dipping the chip in electrolysis liquid, irradiating the nitride chip, and connecting the electrode to a second electrode (Claim 1).

In response to Applicants' previous argument, submitted with Amendment A, that the electrode layer of Pt does not correspond to the claimed step of depositing a thin discontinuous layer of metal on a Group III-V material surface because the layer is a partial coating on a limited area of the chip, the Office Action merely states that the Examiner disagrees "since Peng discloses partially coating the GaN/Group III-V material using the same metal (Pt) as the claimed discontinuous metal layer." Applicants submit that this response does not address the argument put forth in Amendment A, and reassert that the electrode layer does not correspond to the claimed step of depositing a thin discontinuous metal layer. Further, the electrode layer of Peng et al. is a continuous metal structure, not a thin discontinuous metal layer. The term "discontinuous," as used in the present specification and claims, would be understood by one skilled in the art would to mean "not continuous; discrete; lacking sequence or coherence." Since the electrode layer of Peng et al. is continuous, it does not correspond to the thin discontinuous layer as claimed. Further still,

Peng et al. does not disclose nor want a discontinuous layer over the whole chip in order to practice the particular etching method taught in the reference. Thus, Peng et al. does not teach either the feature of depositing a thin discontinuous layer of metal on a Group III-V material surface, or the feature of forming porous Group III-V by etching the Group III-V surface in a HF and oxidant solution.

Przybysz is directed to wet chemical etching of Group III-V in the production of vias or recesses, such as in an integrated circuit. The primary stated goal of Przybysz is to provide an etching solution that is effective for producing predetermined and patterned vias in Group III-V without evolving a gaseous product (col. 1, line 66- col. 2, line 7). This is a device patterning technique, and has nothing to do whatsoever with forming porous Group III-V material. The Office Action states that one skilled in the art would have found it obvious to modify Peng et al. with the etching solution of Przybysz as part of a porous Group III-V formation process. The Examiner has repeatedly stated that the motivation for the modification is that "the amount of F-ion [is] effective to allow sharp uniform etching without precipitation or gaseous evolution at the etching site and the etching solution acts as a particularly effective solvent solution for GaAs/Group III-V material". However, the Examiner has not provided motivation for, nor does Przybysz suggest, the use of wet chemical etching in the formation of porous Group III-V material.

Claim 23 stands rejected under 35 U.S.C. §103(a) as being unpatentable over Peng et al. et al. in view of Yoshikawa (U.S. Patent No. 5,990,605) and further in view of Przybysz. Applicants respectfully traverse and request reconsideration and withdrawal of the

rejection for at least the reasons as stated above, and for at least the additional reason that Yoshikawa does not appear to remedy the deficiencies of Peng et al. and Przybysz.

The Examiner points to the electrode layer in Yoshikawa as corresponding to the claimed step of depositing metal on a Group III-V material surface in a thickness sufficient to prevent nucleation that forms nanometer sized metal particles and small enough to prevent formation of a continuous metal layer. This is incorrect because the standard thin metal contact of Yoshikawa is deposited after the porous semiconductor is formed. In other words, a metal electrode layer is applied only after porous semiconductor is formed by some other method. The claims, by contrast, clearly define that the layer of metal is first deposited on a Group III-V surface and then the Group III-V surface is etched to form the porous Group III-V material. One skilled in the art interpreting claims 1, 12 and 23, having reference to the specification, would readily understand that the claimed method for producing porous Group III-V requires both the depositing and the forming step, and that the step of forming the porous Group III-V by etching the Group III-V surface is not performed before the step of depositing the layer of metal on the Group III-V surface.

As stated in column 1, lines 19-21, the thin metal electrode 15 is formed after the formation of the porous semiconductor layer 13. It is stated that the electron emission device "comprises a semiconductor layer 13 and a thin film metal electrode 15 which are formed, in turn, on a silicon layer 12". This is also emphasized in column 4, lines 58-62 where it is stated once again that the thin metal electrode is layered on the already formed porous silicon semiconductor layer 13. Yoshikawa, therefore, includes no suggestion

whatsoever of the step of depositing a metal on a Group III-V material before the Group III-V material surface is etched to form porous Group III-V, as required in independent claims 1, 12 and 23 in varying scope.

Further, Applicants traverse the rejection of claims 1, 12 and 23 because each of the claims, as originally filed, specifically state "A method for producing porous Group III-V" in its preamble. The Examiner asserted that the preamble is afforded no patentable weight, and has construed the scope of the claims without regard to the meaning of the preamble. As clearly stated in, for example, MPEP § 2111.02, "If the claim preamble, when read in the context of the entire claim, recites limitation of the claim, or, if the claim preamble is 'necessary to give life, meaning, and vitality' to the claim, then the claim preamble should be construed as if in the balance of the claim." The statement, "A method for producing porous Group III-V" clearly intends to give meaning to the claim; i.e., that the steps defined are steps for producing porous Group III-V.

Applicants believe the above to be a complete and sufficient response. Applicants maintain the separate patentability of dependent claims but deem further response unnecessary in view of the above-identified deficiencies in the rejections.

For the foregoing reasons, Applicants believe that this case is in condition for allowance, which is respectfully requested. The Examiner should call applicants' attorney if an interview would expedite prosecution.

Respectfully submitted,

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January 21, 2004

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